ISO9001:2000 Certified SCI Quality System

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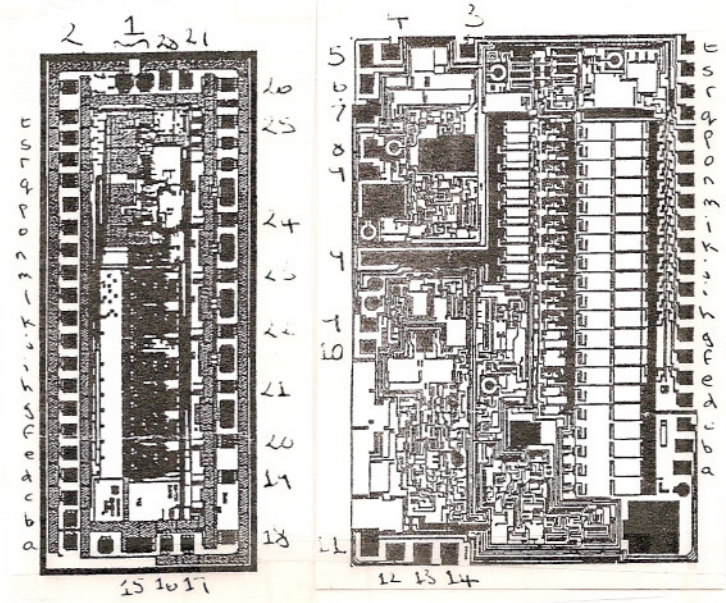
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



E & O E. The supply of dice to this layout can only be guaranteed if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. Tolerance on chip dimensions +/-3 mils.

Approved:	Metallisation/Thickness(KA)	Chip Identification
	Top :	Line Source:
	Back:	Mask Ref :
		Process :
Date:	Back Potential:	Version :
	Man's. Part No:	Geometry :

Chip Dimensions (mils.):	Bond Pads:
Analog 181x121 Digital 178x75	4 x 4 min.

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads : .004 min

APPROVED BY: CB	**DIE SIZE: .181" x .121"**	**DATE: 2/6/01**
MFG: Harris	**THICKNESS: .019"**	**P/N: HIO-0574AA**